UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,693	12/03/2001	Hirotaka Ito	60188-123	6650

7590 06/28/2006

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street N.W.
Washington, DC 20005-3096

EXAMINER	
MATTIS, JASON E	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,693	ITO ET AL.	
	Examiner	Art Unit	
	Jason E. Mattis	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 6-10* is/are rejected.

7)☒ Claim(s) *2 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed 4/11/06. Claims 1-10 are currently pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Aybay et al. (U.S. Pat. 6012116).

With respect to claim 10, Aybay et al. discloses a multi-initiator control method for performing packet-unit communication with each of a plurality of devices connected via a transmission line **(See column 2 line 66 to column 3 line 50, column 4 line 50 to column 5 line 18 and Figures 1-3 of Aybay et al. for reference to a method for controlling access for packet communication between multiple initiator/target units 12-20)**. Aybay et al. also discloses determining whether or not receipt of a command fetch request from one of the plurality of devices is stored **(See column 4**

line 20 to column 5 line 18 and Figures 2-3 of Aybay et al. for reference to determining if a request has been received by one of the units 12-20). Aybay et al. further discloses fetching a command from the one of the plurality of devices and executing the command when it is determined that receipt of a command fetch request is stored **(See column 5 line 55 to column 6 line 5 of Aybay et al. for reference to a target fetching and executing a command from an initiator when the request has been stored)**. Aybay et al. also discloses that the one of the plurality of devices is selected in a predetermined order with the selection being repeated and with the step of determining and fetching being performed for the selected devices **(See column 4 line 20 to column 5 line 18 and Figures 2-3 of Aybay et al. for reference to the selection of the device being done by giving priority to unit 20 over all other units and if unit 20 does not have a request stored selecting one of the devices 12-19 in a round robin manner with the command being fetched for the selected device)**.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-4, and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Nagasaka (U.S. Publication US 2005/0273622 A1) and in further view of Aybay et al.

With respect to claim 1, Applicant's admitted prior art discloses an initiator control unit **(See page 7 lines 21-22 and Figure 11 of Applicant's specification for reference to sequence processor 90, which is an initiator control unit)**. Applicant's admitted prior art also discloses a link core circuit for transmitting a packet to the transmission line and receiving a packet from the transmission line, performing error detection, and outputting the error-detected packet **(See page 7 line 25 to page 8 line 6 and Figure 11 of Applicant's specification for reference to a link core circuit 92 receiving and transmitting packets while performing error detection)**. Applicant's admitted prior art further discloses a packet filter for analyzing the packet received by the link core circuit and outputting the results **(See page 8 lines 9-15 and Figure 11 of Applicant's specification for reference to a packet filter 93 that analyzes the content of packet header fields and sends outputs a signal depending on the result of the analysis)**. Applicant's admitted prior art also discloses a packet processing circuit for generating a packet containing information output by a command control circuit to be transmitted an outputting the packet according to analysis results of the packet filter **(See page 8 lines 11-19 for reference to packet processing circuit 95 generating and outputting a packet according to information received from the packet filter 93)**. Applicant's admitted prior art further discloses a CPU for executing a command contained in the packet **(See Figure 11 of Applicant's admitted prior art**

for reference to CPU 31, which executes a command as output by the packet processing circuit 95). Applicant's admitted prior art does not disclose that the control unit is a multi-initiator control unit. Applicant's admitted prior art also does not disclose a plurality of command control circuits for controlling a command processing sequence. Applicant's admitted prior art further does not disclose a multi-control circuit for giving sequence execution permission to one of the command control circuits.

With respect to claim 1, Nagasaka, in the field of communications, discloses a multi-initiator control unit having a plurality of command control circuits for controlling a command processing sequence **(See page 5 paragraphs 60-64 and Figure 1 of Nagasaka for reference to a target device that can have more than one logical unit, which is a command control circuit, with each logical unit being able to service at least one initiator at a time)**. A multi-initiator control unit having a plurality of command control circuits for controlling a command processing sequence has the advantage of allowing a target device to be able receive commands from more than one initiator at the same time.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Nagasaka, to combine a multi-initiator control unit having a plurality of command control circuits for controlling a command processing sequence, as suggested by Nagasaka, with the system described by the Applicant's admitted prior art, with the motivation being to allow a target device to be able receive commands from more than one initiator at the same time.

With respect to claim 1, Aybay et al., in the field of communications discloses a multi-control circuit for giving sequence execution permission to one of a plurality of command control circuits **(See column 2 line 66 to column 3 line 50, column 4 line 50 to column 5 line 18 and Figures 1-3 of Aybay et al. for reference to bus interface unit (BIU) 11, which is a multi-control circuit that gives sequence execution permission to one of a plurality of control units located in units 12-20)**. Using a multi-control circuit for giving sequence execution permission to one of a plurality of command control circuits has the advantage of allowing arbitration of the use of the shared target resource to be controlled such that each device may access the target resource in a fair and predetermined manner.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Aybay et al., to combine using a multi-control circuit for giving sequence execution permission to one of a plurality of command control circuits, as suggested by Aybay et al., with the system described by the Applicant's admitted prior art and Nagasaka, with the motivation being to allow arbitration of the use of the shared target resource to be controlled such that each device may access the target resource in a fair and predetermined manner.

With respect to claim 3, Applicant's admitted prior art does not disclose that the command control circuits store information in a command fetch request packet and performs the command fetch operation once execution permission is given.

With respect to claim 3, Nagasaka discloses that the command control circuits store information in a command fetch request packet transmitted from the

corresponding device **(See page 5 paragraph 64 for reference to the logical unit having a fetch agent (FE) that is used to store command fetch request packets transmitted from initiator devices)**. Having command control circuits store information in a command fetch request packet transmitted from the corresponding device has the advantage of allowing multiple initiator to send commands at the same time to multiple logical units of the same target device.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Nagasaka, to combine having command control circuits store information in a command fetch request packet transmitted from the corresponding device, as suggested by Nagasaka, with the system described by the Applicant's admitted prior art, with the motivation being to allow multiple initiator to send commands at the same time to multiple logical units of the same target device.

With respect to claim 3, Aybay et al. discloses performing a command fetch operation for a device once the sequence execution permission is given to the command control circuit by the multi-control circuit **(See column 5 line 55 to column 6 line 5 of Aybay et al. for reference to a target fetching and executing a command from an initiator when initiator has been selected and given execution permission)**. Performing a command fetch operation for a device once the sequence execution permission is given to the command control circuit by the multi-control circuit has the advantage of allowing commands to be fetched and executed by a target device such that each device may access the target resource in a fair and predetermined manner.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Aybay et al., to combine performing a command fetch operation for a device once the sequence execution permission is given to the command control circuit by the multi-control circuit, as suggested by Aybay et al., with the system described by the Applicant's admitted prior art and Nagasaka, with the motivation being to allow commands to be fetched and executed by a target device such that each device may access the target resource in a fair and predetermined manner.

With respect to claim 4, the Applicant's admitted prior art does not disclose the command control circuits receiving a command fetch request during execution of a data transfer processing sequence.

With respect to claim 4, Aybay et al. discloses that command fetch requests may be received during execution of a data transfer processing sequence **(See column 2 line 66 to column 3 line 50 and Figure 1 of Aybay et al. for reference to the request being sent to the BIU on data lines 12a-20a that are separate from the bus used to transfer data, such that request may be sent even as data is being processed and transferred)**. Allowing command fetch requests to be received during execution of a data transfer processing sequence has the advantage of allowing the processing of commands to be performed more quickly since commands to not have to wait for data processing and transfer of a pervious command to finish before being sent.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Aybay et al., to combine allowing command

fetch requests to be received during execution of a data transfer processing sequence, as suggested by Aybay et al., with the system described by the Applicant's admitted prior art and Nagasaka, with the motivation being to allow the processing of commands to be performed more quickly since commands to not have to wait for data processing and transfer of a pervious command to finish before being sent.

With respect to claim 6, the Applicant's admitted prior art does not disclose the multi-control circuit selecting one of the plurality of devices in a predetermined order every time a command processing sequence is terminated and giving permission to execute the selected device command.

With respect to claim 6, Aybay et al. discloses selecting one of the plurality of devices in a predetermined order every time a command processing sequence is terminated and giving permission to execute the selected device command **(See column 4 line 20 to column 5 line 18 and Figures 2-3 of Aybay et al. for reference to the selection of the device being done as soon as a previous command processing sequence has ended)**. Selecting one of the plurality of devices in a predetermined order every time a command processing sequence is terminated and giving permission to execute the selected device command has the advantage of making sure that the shared target resource is used as quickly as possible once the resource is available.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Aybay et al., to combine selecting one of the plurality of devices in a predetermined order every time a command processing

sequence is terminated and giving permission to execute the selected device command, as suggested by Aybay et al., with the system described by the Applicant's admitted prior art and Nagasaka, with the motivation being to make sure that the shared target resource is used as quickly as possible once the resource is available.

With respect to claim 7, Applicant's admitted prior art discloses a transfer control circuit for controlling data transfer between the packet processing circuit and the outside of the control unit **(See page 8 lines 15-19 of Applicant's specification for reference to the transfer control circuit 96)**. Applicant's admitted prior art also discloses that the packet processing circuit retrieves data and outputs data to the transfer control circuit and also generates a packet containing data transferred to the transfer control circuit and outputs the packet to the link core circuit **(See page 8 lines 15-21 for reference to the packet processing circuit 95 performing this process)**.

With respect to claim 8, Applicant's admitted prior art does not disclose that the CPU is allowed to give sequence execution permission.

With respect to claim 8, Aybay et al. discloses that a CPU is allowed to give sequence execution permission **(See the Abstract and Figure 2 of Aybay et al. for reference to BIU 11, which gives sequence execution permission being located in a CPU)**. Allowing a CPU to give sequence execution permission has the advantage of allowing the device in control of the target resource to be the same device that decides which initiator may next use the target resource.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Aybay et al., to combine allowing a CPU to

give sequence execution permission, as suggested by Aybay et al., with the system described by the Applicant's admitted prior art and Nagasaka, with the motivation being to allow the device in control of the target resource to be the same device that decides which initiator may next use the target resource.

With respect to claim 9, the Applicant's admitted prior art does not disclose that correspondence is established between the node number of each of the devices and the position of a bit field for identification of the node number.

With respect to claim 9, Aybay et al. discloses establishing a correspondence between the node number of each of the devices and the position of a bit field for identification of the node number (See column 4 lines 20-35 of Aybay et al. for reference to each request including bits identifying the initiator unit that sent the request, meaning there is a correspondence between the number of an initiator unit and position of a bit field in the request). Establishing a correspondence between the node number of each of the devices and the position of a bit field for identification of the node number has the advantage of allowing requests to be sorted by the device making the requests.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Aybay et al., to combine establishing a correspondence between the node number of each of the devices and the position of a bit field for identification of the node number, as suggested by Aybay et al., with the system described by the Applicant's admitted prior art and Nagasaka, with the motivation being to allow requests to be sorted by the device making the requests.

Allowable Subject Matter

6. Claims 2 and 5 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed 4/11/06 have been fully considered but they are not persuasive.

In response to Applicant's argument that:

> "Applicants submit that Aybay et al. does not disclose a multi-initiator control method including, among other things, the step of determining whether or not receipt of a command fetch request from one of the plurality of devices is stored, as recited in claim 10." (See page 2 of Applicant's Remarks section)

the Examiner respectfully disagrees. Aybay et al. discloses that requests from initiators are received and decoded (See column 4 lines 20-24 of Aybay et al.). In order to receive and decode a request from an initiator, the request must be somehow stored in the BIU 11. Aybay et al. also discloses that an arbitration process is used to arbitrate among present request and grant a winning request (See column 4 lines 50-52 of Aybay et al.). Aybay et al. further discloses that initiator units 12-20 are polled in a

predetermined manner to determine whether they have made a request (See column 4 lines 59-65. The result of this polling process is a determination that an initiator has a request stored that is waiting to be acted on and storing an address indicator, which is the storage location, of the winning request. Therefore, through the polling process, Aybay et al. does disclose, "determining whether or not receipt of a command fetch request from one of the plurality of devices is stored", as claimed.

In response to Applicant's argument that:

> "The AAPA and Nagasaka, either individually or in combination, do not disclose or teach a multi-initiator unit including, among other things, a plurality of command control circuits for controlling a command processing sequence performed with the corresponding device, as recited in independent claim 1." (See page 4 of Applicant's Remarks section)

the Examiner respectfully disagrees. While it is true that Nagasaka does discuss at length an embodiment of a target device including one logical unit, Nagasaka does not limit the disclosed target unit from having more than one logical unit. In multiple instances Nagasaka disclose that a target device may have more than one logical unit (See page 1 paragraphs 7-9, page 2 paragraphs 20-21, page 4 paragraph 53, page 5 paragraph 63, and page 12 paragraph 158 for instances where Nagasaka disclose a target device having multiple logical units). Therefore, Nagasaka does disclose a target device having a plurality of control circuits as claimed.

In response to Applicant's argument that:

"Applicants further submit that there is no motivation to modify the AAPA based on the teachings of Nagasaka to arrive at the claimed invention."

(See page 5 of Applicant's Remarks section)

the Examiner respectfully disagrees. The motivation used in the rejections above to combine multiple command control circuits, as discloses by Nagasaka, with the Applicant's admitted prior art is that multiple command control circuits allow a target device to be able receive commands from more than one initiator at the same time. This motivation may be found in the Nagasaka reference itself. Nagasaka discloses that the use of multiple logical units allows a plurality of initiators to share a target (See page 4 paragraph 53 of Nagasaka for reference to this advantage). Since the motivation to combine is found in the Nagasaka reference itself, the combination of references used in the rejections above is proper.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E. Mattis whose telephone number is (571) 272-3154. The examiner can normally be reached on M-F 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jem

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600